Amendments to the Drawings

The attached sheet of drawings includes a change to Fig. 2. This sheet, which includes Fig. 2, replaces the original sheet including Fig. 2. In Fig. 2, the label of the bottom microprocessor has been changed from "(P(n-1))" to –(P(m-1))--.

Attachment: Replacement sheet

REMARKS

In Response to the Office Action mailed November 22, 2006, applicants respectfully request reconsideration. In the Office Action, claims 5-12, 18-24, 26 and 27 were objected to and claims 1-4, 13-17, 25 and 28-31 were rejected. By this amendment, the Specification, Fig. 2 and claims 1 and 28 have been amended. Claims 1-31 remain pending in this application.

Rejection Under 35 U.S.C. §112

Claims 28-31 were rejected under 35 U.S.C. §112 as being indefinite. Regarding claim 28, the examiner stated that the relationships between the steps were unclear, that the term "an access arbitration signal" could not be ascertained and that the language "arbitrating access to the particular processor" could not be understood.

Claim 28 and the Specification have been amended to make claim 28 more clear. Step D of claim 28 was amended to indicate that the access indication signal received in Step D is in addition to the access indication signals received in Step A. Step E was amended to indicate that access is arbitrated to the shared resource by the particular processor. The specification was amended to specify that the output of the OR gate 37 is the "access arbitration signal." Support for this amendment is found in the claims and in the Summary. No new matter has been added.

Regarding claims 29 and 30, the examiner states that the language "granting access to the shared resource by the particular processor" and "blocking access to the shared resource by the particular processor" is not understood, since the arbiter is used to grant or block access to the shared resource, not the processor.

This rejection is respectfully traversed. First, there is no arbiter recited in claims 28-31. Second, based on the amendment to claim 28, it is clear that, in Step E, access *to the shared resource* is arbitrated and that access to the shared resource is carried out *by the particular processor.* Therefore, in claim 29 it is clear that it is not the processor that

is granting access to the shared resource, but that the access that is granted is carried out by the processor. Likewise, in claim 30 it is clear that it is not the processor that is blocking access to the shared resource, but that the access that is blocked is access that would have been carried out by the processor.

Based on these amendments, applicants assert that claims 28-31 are definite and that the rejection of claims 28-31 under 35 U.S.C. §112 is moot and should be withdrawn.

Claim Rejection Under 35 U.S.C. §102

Claims 1-4, 13-17, 25 and 28-31 were rejected under 35 U.S.C. §102 as being anticipated by Derrick et al. This rejection is respectfully traversed, as Derrick does not teach every element of the claims, as is required for a proper rejected under 35 U.S.C. §102.

Amended independent claim 1 recites a system for arbitrating access to a shared resource comprising:

a plurality of microprocessors;

a shared resource; and

a controller coupled to the plurality of microprocessors and the shared resource by a first bus and a second bus, respectively, the controller including a register having a lock portion associated with each of the plurality of processors and a status portion, each of the lock portions indicating whether the associated one of the plurality of microprocessors has obtained access to communicate with the shared resource, and the status portion includes a bit indicating whether any of the plurality of microprocessors has obtained access to communicate with the shared resource.

Derrick teaches a semaphore access control buffer which controls access to semaphores by multiple devices. The buffer includes a number of registers 520, Fig. 5, each being adapted to hold data pertaining to one of the semaphores. The data includes the address of the semaphore, whether or not the resource associated with the semaphore is owned by a device and the ID of the device that owns the resource. See column 4, line

66 – column 5, line 8. Each semaphore has a specific register 520 associated with it, the contents of which a device desiring access must read in order to determine whether the semaphore/resource is available to be accessed by the device. If, upon reading the register, the device determines that the resource is not owned by another device, the device writes to the lock bit/ID of the register 520 to take ownership of the resource. Column 5, lines 41-48.

As set forth in claim 1, the system of the present invention includes, among other features, a register having a lock portion associated with each of the plurality of processors. To the contrary, the device of Derrick has a register associated with each of the semaphores/resources. Derrick does not teach or suggest a lock portion associated with each of a plurality of processors. In fact, Derrick only teaches a memory location in the register in which a lock bit is written if a device takes ownership of the semaphore/resource associated with the particular register assigned to the semaphore.

While the examiner states that Derrick teaches ID fields associated with each processor, this is not the case. As stated above, each register 520 includes an ID field for the identification of the master that currently owns the associated resource. However, when that master no longer owns that resource, and a different master takes ownership, that ID field then includes the identification of the new master. Therefore, the ID field in each register is not associated with each processor, as the information in that field can identify any of the masters that take ownership of the resource associated with the register. Column 5, lines 34-52.

Accordingly, since Derrick does not teach every element of independent claim 1, the rejection of independent claim 1 is improper and should be withdrawn. Therefore, independent claim 1 is allowable over the art of record.

Claims 3-12 depend from independent claim 1 and are allowable for at least the same reasons as independent claim 1.

Independent claim 13 recites a controller for arbitrating access to at least one shared resource by a plurality of processors, the controller comprising:

a first register portion including a plurality of layers, each of the plurality of layers being associated with a different one of the plurality of processors, each of the

plurality of layers including an access indication portion associated with each of the at least one shared resource, the access indication portion holding an indicator of whether a processor associated with a particular layer has obtained access to communicate with the shared resource associated with the access indication portion of the particular layer; and

an access arbitration device associated with all of the access indication portions of each of the at least one shared resources for controlling access to the associated shared resource by the plurality of processors, the access arbitration device including an input for receiving access indication signals from the plurality of processors, the access arbitration device:

(A) determining whether the at least one shared resource is being accessed by any of the plurality of processors; and

(B) arbitrating access to the shared resource based on the determination made in Step (A).

As set forth above, Derrick does not teach a first register portion including a plurality of layers, each of the plurality of layers being associated with a different one of the plurality of processors. There is no disclosure in Derrick that teaches or suggests that any part of the spin buffer 502, which includes registers 520, is associated with a different one of the masters that seek ownership of the semaphores. In Derrick's system, each register 520 is associated with a different semaphore, but no registers are associated with a different master.

Furthermore, Derrick does not teach or suggest an access indication portion which holds an indicator of whether a processor associated with a particular layer has obtained access to communicate with the shared resource associated with the access indication portion of the particular layer. The examiner states that the access indication portion of Derrick is the ID field, however, as discussed above, the ID field is a part of the register which is associated with a semaphore.

Derrick also does not teach an access arbitration device associated with all of the access indication portions for carrying out the steps recited in the claim. While Derrick does disclose an arbiter 506, as pointed out by the examiner, there is absolutely no description in Derrick of the operation of the arbiter. Therefore, the examiner cannot

attribute the operation of the access arbitration device recited in claim 13 to the arbiter of Derrick because there is no support in Derrick that would even remotely suggest that the arbiter 506 performs the steps recited in claim 13. On several occasions in the rejection, the examiner states that it is clear that the Derrick arbiter is performing the steps and receiving the inputs recited as being performed and received by the access arbitration device in claim 13, but the examiner does not specifically point out where in Derrick these features are taught. In order to enable the applicants to fully understand the rejection, the applicants request that the examiner specifically point out where in the Derrick disclosure the features and functions of the access arbitration device recited in claim 13 are taught.

Accordingly, since Derrick does not teach every element of independent claim 13, the rejection of independent claim 13 is improper and should be withdrawn. Therefore, independent claim 13 is allowable over the art of record.

Claims 14-27 depend from independent claim 13 and are allowable for at least the same reasons as independent claim 13.

Independent claim 28 recites a method of arbitrating access to a shared resource by a plurality of processors, the method comprising:

A) processing access indication signals received from each of the plurality of processors;

B) storing the processed access indication signals;

C) performing a logic operation on the processed access indication signals to generate an access arbitration signal;

D) receiving a further access indication signal from a particular one of the plurality of processors; and

E) arbitrating access to the shared resource by the particular processor based on the state of the access arbitration signal.

As set forth above, Derrick does not teach processing access indication signals received from each of a plurality of processors. While individual masters may read a register associated with a semaphore, there is no access indication signal in the Derrick

system that is received from the masters and then processed by the system. Since there are no access indication signals in Derrick's system, they cannot be stored.

Derrick does not teach performing a logic operation on the processed access indication signals to generate an access arbitration signal. Since, as discussed above, Derrick does not teach access indication signals, he cannot teach performing a logic operation on them, nor can he teach receiving a further access indication signal from a particular one of the plurality of processors. Lastly, since no operation of the arbiter 506 is disclosed by Derrick, Derrick does not teach or suggest arbitrating access to the shared resource by the particular processor based on the state of the access arbitration signal.

Accordingly, since Derrick does not teach every element of independent claim 28, the rejection of independent claim 28 is improper and should be withdrawn. Therefore, independent claim 28 is allowable over the art of record.

Claims 29-31 depend from independent claim 28 and are allowable for at least the same reasons as independent claim 28.

Amendments to the Specification

Applicants made amendments to the specification to clear up minor typographical errors. No new matter has been added.

Amendment to the Drawings

Applicant amended Fig. 2 to correct a typo. In amended Fig. 2, the label of the bottom microprocessor has been changed from "(P(n-1))" to –(P(m-1))--.

Based on the foregoing, applicants respectfully assert that claims 1-31 are allowable over the art of record and respectfully request that a timely Notice of Allowance be issued in this application.

In the event the Patent Office deems personal contact desirable in disposition of this matter, the Office is invited to contact the undersigned attorney at (508) 293-7835.

Applicants submit herewith a Request for One Month Extension of Time under 37 C.F.R. §1.136(a). Please charge any additional fees occasioned by this submission to Deposit Account No. 05-0889.

Respectfully submitted,

Dated: 3/22/06

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